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13. ABSTRACT (Maximum 200 words) The aim of this research project was to alleviate the tone problem in sigma delta modulators by exploiting chaos and unstable limit cycles. This was achieved by designing encoders with open loop poles outside the unit circle. A side effect of this approach is the possibility of the modulator becoming unstable, i.e., of the internal states becoming unbounded. An analysis of the stability characteristics and the tonal properties of the chaotic double loop sigma delta modulator was presented. Bounds on maximum internal states were determined. It was shown that the tone behavior of the double loop sigma delta modulator is improved when the poles are moved outside the unit circle; however, not all spectral peaks are removed. A mechanism for tone generation was identified and general spectral characteristics as a function of pole location were obtained. It was shown that there is a trade-off between stability, tonal behavior and signal-to-noise ratio performance. Audio testing along with a series of simulations were also performed to compare the efficacy of pole placement with that of the more traditional tone removal technique of dithering. Based on the results, design guidelines were presented. In addition to the above results, a switched-capacitor implementation of the double loop sigma delta modulator with open loop poles outside the unit circle was considered. Initial testing of the integrated circuit verified some of the theoretical results on the tonal behavior of the double loop sigma delta modulator.				
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1 Introduction

The occurrence of tones is a persistent problem in sigma delta modulators. Repeating patterns at the output of sigma delta modulators result in spectral peaks or tones in the output spectrum. Tones are especially objectionable in audio applications since their presence in the signal baseband may result in audible disturbances.

For a given sigma delta structure, the tone behavior may be improved by making the dynamics of the modulator chaotic. This is achieved by moving its open loop poles outside the unit circle. All limit cycles of the chaotic modulator are unstable, thus precluding spectral peaks caused by stable periodic motion in the state space. A side effect of this method is the possibility of the modulator becoming unstable, i.e. of the internal states becoming unbounded.

The focus of this research was on studying the pole placement approach, as applied to the double loop sigma delta modulator. Contributions were made in characterizing state space trajectories, obtaining bounds on internal signal levels, and describing the tone behavior. These results were used to provide design guidelines for pole placement. A practical implementation of the above tone removal technique using the switched capacitor technology was also considered.

The analysis and simulations in this project assumed constant encoder input. This assumption has been widely used in the literature [1, 2, 3]. It follows from the fact that the input to the modulator is oversampled and therefore may be approximated by a constant over large time intervals. In addition, it has been shown that the tone behavior is worse when the input to the modulator is constant or slowly varying.

2 Saturation Properties

A block diagram of the double loop sigma delta modulator is shown in Figure 1 in the appendix at the end of this report. Stability or saturation was shown to be an important concern in the design of the double loop sigma delta modulator with poles outside the unit circle. Stability of the internal states was determined by analyzing the steady state behavior of two continuous time approximations to the double loop modulator. The steady state behavior of the first continuous time approximation provided a saturation measure on the internal states. Properties of solutions to differential equations were used to prove that when the continuous time system exhibits an unstable limit cycle, then the limit cycle provides an *unboundedness boundary* for the states of the double loop modulator. Specifically, it was shown that discrete time trajectories outside this boundary will remain outside and will grow to infinity. Thus, the unboundedness boundary was used to check for unboundedness of the discrete time trajectories.

In contrast, and complimentary to, the first continuous time approximation, a second continuous time approximation was obtained whose properties provided a bound on the maximum signal levels. Analysis of the trajectories in the phase plane showed that a closed orbit of the second continuous time approximation provides a trapping region for

the states of the double loop modulator. Specifically, simulations and analysis determined that once inside the trapping region, a trajectory of the double loop modulator remains inside and exhibits unstable but bounded behavior. Thus, all initial conditions inside the trapping region were shown to result in bounded behavior. Detailed derivation and analysis of the unboundedness boundary and the trapping region are given in [4, 5, 6].

3 Input Dynamic Range and Signal-to-Noise Ratio Performance

The effect of the system parameters on the stability boundaries was studied. It was shown that the trapping region is inside the unboundedness boundary. The unboundedness boundary shrinks in the vertical direction and approaches the trapping region as the dc input is increased and the poles are fixed outside the unit circle. Similar results were observed when the input was fixed and the pole moduli were increased. This indicated a loss in allowable input dynamic range. Table 1 in the appendix summarizes the effect of pole location on the maximum allowable input dynamic range.

The effect of pole location on signal-to-noise ratio performance was also considered. It was shown that moving the open loop poles outside the unit circle not only reduces the dynamic range but also degenerates the noise shaping characteristics of the sigma delta modulator, thus resulting in a loss in signal-to-noise ratio performance. These results are summarized in Figure 2 of the appendix. Detailed derivation of the above results are presented in [4, 5, 6].

4 A Mechanism for Tone Generation

The tonal behavior of the double loop sigma delta modulator with poles outside the unit circle was considered. It was found that while pole placement outside the unit circle improves the tone behavior, it does not completely remove idle tones. A mechanism for tone generation in the double loop modulator with open loop poles outside the unit circle was identified. Specifically, steady state analysis in the neighborhood of unstable limit cycles indicated that for some unstable limit cycles, referred to as *dominant* unstable limit cycles, periodicity and therefore tones occur because the internal states persistently move from the *neighborhood* of one point on the limit cycle to the *neighborhood* of another point on the limit cycle. This steady state behavior was shown to result in an output bit sequence that is periodic with intermittent breaks in periodicity, thus resulting in tones in the output spectrum. A numerical technique to identify dominant unstable limit cycles and approximate the boundaries of the attractor in their neighborhood was developed. Details of these results are given in [5, 6, 7].

5 Tonal Behavior

General spectral characteristics as a function of pole location and constant input value were determined. Simulations and analysis indicated that for a given dc input value, the location of tones is intimately related to the pole modulus of the first integrator, while the relative power of various tones is a function of both integrator poles. Details of the results discussed in this section may be found in [6, 8, 9].

5.1 Spectral Characteristics

For the case where one open loop pole is fixed on the unit circle while the other is allowed to move outside the unit circle, the location of possible spectral peaks in the output periodograms were determined to within an integer multiple.

For the case where both open loop poles are moved outside the unit circle, the sample mean of the output bit sequence was determined to be approximated by the product of the first open loop pole with the dc input value. Furthermore, it was shown that the dominant output pattern consisted of the shortest possible bit pattern with an average value that is the product of the first integrator pole with the dc input, and with evenly distributed +1's and -1's. These results along with extensive simulations of the output periodogram were used to determine the frequency location of two dominant spectral peaks, denoted by fb and fh , as a function of the open loop poles and dc input values. Frequency location fb is given by the product of the sample mean of the output bit sequence with the sampling frequency, and frequency location fh is the difference between half the sampling frequency and the product of the sample mean of the output bit sequence with half the sampling frequency.

For example, applying the analysis discussed in the previous paragraph to the double loop modulator with a dc input of 0.198, and poles at 1.01, and 1.03 yields that the dominant output bit pattern is $b = (1, -1, 1, -1, 1)$. This result is in agreement with simulations of the output bit sequence shown in Figure 3 in the appendix. Figure 3 (a) shows the output bit sequence for 120 time steps. The regions separated by vertical dashed lines and labeled 1, 2 and 3 in Figure 3 (a) contain portions of the output bit sequence that coincide with pattern b . More generally, it was found that the percentage of occurrence of pattern b in the output bit sequence was 65%. Figure 3 (b) in the appendix shows the output periodogram obtained by averaging over 20 Discrete Fourier Transforms each 60,000 points long. The output periodogram contains dominant tones at fb and fh , denoted by \times and \circ in Figure 3 (b), respectively. These tones are in agreement with the dominant frequencies of pattern b .

5.2 General Trends

It was shown that for dc inputs near zero, frequency location fb corresponds to the first spectral peak, while frequency location fh corresponds to the last spectral peak, i.e.,

to the peak closest to half the sampling rate. Specifically, simulations of the output periodogram indicated that dc inputs less than or equal to 0.031 (0.05) result in spectra whose lowest (highest) frequency peaks are located at fb (fh).

For a given oversampling ratio and sufficiently small dc input, the spectral peak located at fb was shown to fall in the signal baseband. The relative amplitude of this tone was studied as a function of pole location. The amount of tone suppression near dc was determined to be a function of the location of the real-valued integrator poles. As pole moduli outside the unit circle are moved toward the unit circle, the noise shaping properties are improved thus reducing the level of low frequency peaks. These results are illustrated in Figure 4 in the appendix. Figure 4 shows the relative amplitude of the tone at fb as a function of pole location, for dc input values 0.0011, 0.0019, 0.004 and 0.0078. These values are chosen to be the largest dc inputs for which frequency location fb occurs at the edge of the baseband for the oversampling ratio of 512, 256, 128 and 64, respectively.

For dc input values 0.0011, 0.0019, and 0.004, in Figure 4, the amplitude of the tone at fb initially increases as pole values are increased from 1.005 to 1.05 and then decreases as the poles are further increased beyond 1.05. On the other hand, the allowable input dynamic range and signal-to-noise ratio are reduced monotonically as the pole values increase from 1.005 to 1.08. For instance, for pole values greater than 1.08, the maximum allowable input that results in bounded internal behavior was found to be less than 0.2.

As seen in Figure 4, keeping both poles close to but slightly outside the unit circle, such as 1.005, becomes less effective in suppressing the lowest frequency tone as larger inputs are considered. For instance, moving the poles from 1.02 to 1.005 reduces the level of the tone at fb by approximately 6 dB when the input is 0.0019, by approximately 3.5 dB when the input is 0.003, and by 2 dB when the input is 0.004, but, increases by approximately 1 dB when the dc input is 0.0078. For the dc input of 0.0078, the level of the tone at fb decreases monotonically as poles are increased beyond 1.01, with a sharp decrease occurring beyond 1.07.

The study of the relative amplitude of the first spectral peak for various pole locations and oversampling ratios suggested that for oversampling ratios greater than or equal to 256, baseband tone suppression may be achieved for pole values slightly outside the unit circle, such as 1.005. This, however, is not the case when considering smaller oversampling ratios, such as 64. Indeed, for the oversampling ratio of 64 much larger pole values such as 1.08 are needed in order to reduce the level of baseband tones. However, such large values of poles were shown to result in a significant drop in the signal-to-noise ratio performance.

It was also suggested that besides keeping both open loop poles close to, but outside, the unit circle, another way to suppress low frequency tones while increasing 'randomness' in state space trajectories is to keep one pole close to, and move the other farther away from, the unit circle.

6 A Comparison of Pole Placement with Dithering

A series of simulations were performed to compare the performance of the pole placement technique with that of the more traditional tone removal technique of dithering. Results were obtained for the oversampling ratio of 256. Audio testing was also performed in order to evaluate audible distortion as a function of tone amplitude. The results presented in this section are discussed in detail in [6, 8, 9].

6.1 Experimental Set-up

The set-up used for audio testing consisted of a Crystal Semiconductor evaluation board, CS4303, which includes a digital interpolation filter followed by a sigma delta modulator, a return-to-zero type one bit digital-to-analog converter and analog low-pass post filters. The board was modified by adding a switch, S , to its hardware enabling it to accept computer generated bit streams. The off position of the switch corresponds to the normal operation of the evaluation board, while the on position allows for the output bit stream from simulations of a sigma delta modulator to be used as the input to the one bit digital-to-analog converter. Specifically, the on position of the switch allows for a computer simulated bit stream, that has first been stored in a buffer, to be played out into the one bit digital-to-analog converter followed by the analog low pass post filter of the Crystal Semiconductor evaluation board. The output of the analog post filter was played into a set of speakers, with bandwidth up to 15KHZ, as well as a wideband spectrum analyzer. A block diagram of this set-up is shown in Figure 5 of the appendix.

Experiments done on the Crystal evaluation board indicated that output periodograms containing baseband tones that are 4 dB above the noise floor result in *audible* tones, while those containing tones below 4 dB are not discernible. Furthermore, this set up did not exhibit baseband tones caused by intermodulation of high frequency peaks. these results were used in the evaluation of the dithered modulator and the modulator with unstable filter dynamics as discussed below.

6.2 Results

The comparison between pole placement and dithering was performed by estimating peak signal-to-noise values for the double loop modulator with various dither signals and pole locations. Tonal behavior of the modulators with similar signal-to-noise performances was then compared. This was done by evaluating baseband tonal behavior on a grid of dc input values. Three commonly used dither signals were considered, namely, continuously random dither signals, 1-bit quantized random dither signals, and 8-bits quantized random dither signals, each with peak-to-peak amplitudes of 1, and uniform probability distribution functions. As discussed in Section 5, poles slightly outside the unit circle perform 'best' in terms of low frequency tone removal and signal-to-noise ratio performance when large oversampling ratios such as 256 are considered. Thus, the comparison

between the pole placement technique and dithering was performed for the oversampling ratio of 256.

Both pole placement and dithering removed audible tones. Specifically, for pole values close to the unit circle at 1.005, baseband tones did not exceed 1 dB above the noise floor. Here, the loss in peak signal-to-noise ratio as compared to the ideal double loop modulator was 4 dB. The dithered double loop modulator with continuously random dither and 8-bits quantized dither resulted in similar baseband tone behavior with a loss of 6 dB in peak signal-to-noise ratio. The 1 bit quantized dithered modulator was free of baseband tones. However, the loss in signal-to-noise ratio was found to be 10 dB.

In terms of hardware implementation for analog-to-digital conversion applications, the addition of a dither source has been found to introduce more complexity than pole placement. Whereas extra analog hardware is needed to implement a random noise source for the dithered modulator, pole placement outside the unit circle may be achieved by either appropriately designing capacitor ratios in the integrators or by applying positive feedback in the op amps [10]. The complexity in generating random dither signals for analog-to-digital applications may be reduced by quantizing the dither signal to 1 bit [11]. However, this resulted in a large loss in signal-to-noise ratio performance.

7 Alternative Tone Removal Techniques

It was also found that neither pole placement nor additive dither remove all high frequency tones. High frequency peaks may fold into the signal baseband due to circuit nonlinearities when non-return-to-zero type digital-to-analog converters are used in digital-to-analog conversion applications [12].

Two procedures based on error diffusion halftoning techniques and aimed at suppressing high frequency tones were investigated. Specifically, a double loop sigma delta modulator with time varying poles, and an error diffusion structure whose noise transfer function contained a zero near -1 were considered. The former technique was aimed at yielding broadband spectra, while the latter was directed toward removing high frequency tones which are near half the sampling rate. It was found that more broadband spectral characteristics are obtained using these methods at the expense of an extensive loss in signal-to-noise ratio performance. Details of these results are given in [6].

8 Hardware Implementation

The design of a fully differentiable double loop sigma delta modulator with unstable filter dynamics used for audio applications was considered [10]. This design was implemented using the switched-capacitor technique. The open loop poles of the modulator were moved outside the unit circle by applying positive feedback around the the operational amplifiers.

The experimental results consisted of acquiring and storing the bit stream at the output of the sigma delta modulator in a computer. This allowed for the evaluation of the output periodogram using the stored output bit stream.

Initial testing of the integrated circuit verified the existence and frequency location of dominant spectral peaks as discussed in Section 5 of this reports. A design flaw prevented the complete evaluation of the tonal behavior of this implementation. This flaw is being fixed. The improved design will be tested once completed.

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Appendix:

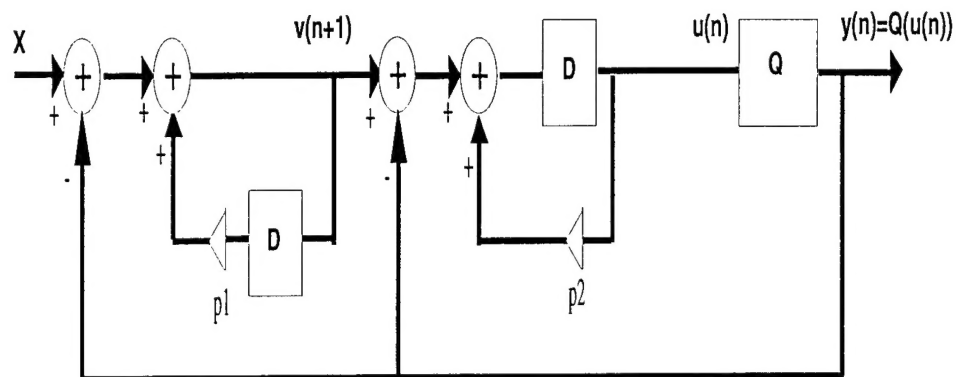


Figure 1: *Double Loop $\Sigma\Delta$ Modulator*

$p_1 = p_2$	X
1.02	.8
1.03	.8
1.04	.7
1.06	.5
1.08	.2
1.09	0

Table 1: *Maximum allowable input X for a given $p_1 = p_2$.*

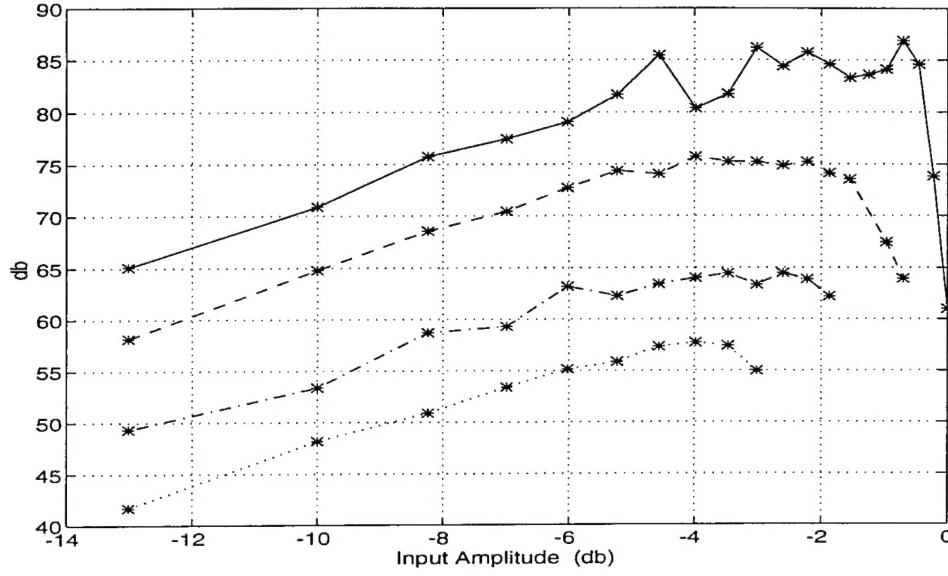


Figure 2: *Signal-to-noise ratio vs. input amplitude for an oversampling ratio of 64. Top curve: $p = p_1 = p_2 = 1$, curve below: $p = 1.02$, curve below: $p = 1.04$, curve below: $p = 1.06$.*

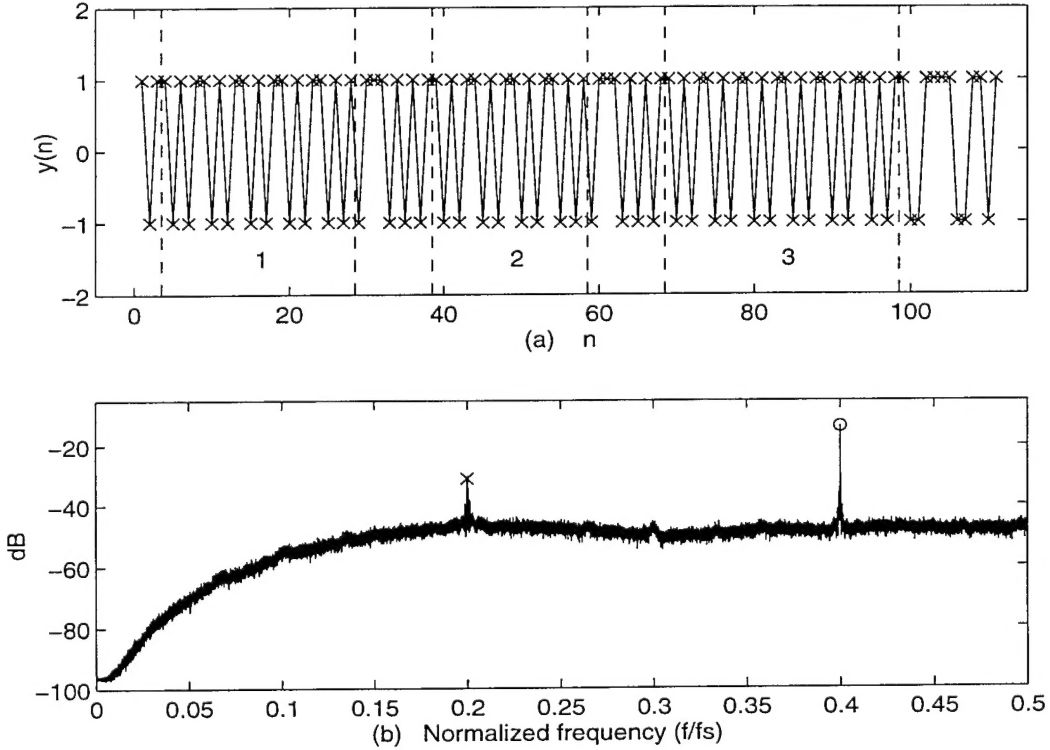


Figure 3: $X = 0.198$, $(p_1, p_2) = (1.01, 1.03)$. (a) *Output bit sequence (time domain).* (b) *Output periodogram; \times : frequency location f_b , o : frequency location f_h .*

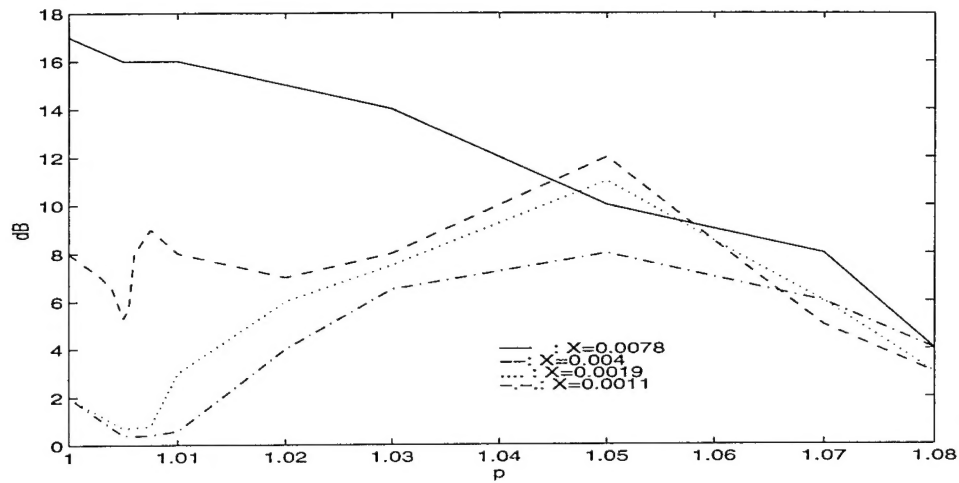


Figure 4: *Relative amplitude of the tone at fb as a function of open loop poles, $p = p_1 = p_2$.*

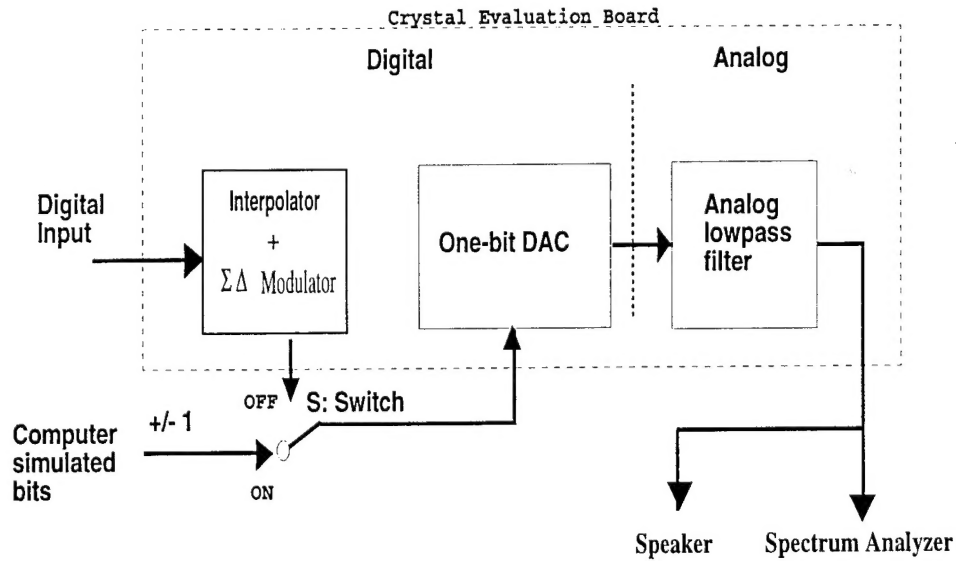


Figure 5: Block diagram of the experimental set-up used in audio testing.